A Low-Voltage 5-GHz Quadrature Up-Conversion Mixer for Wireless Transmitter

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Abstract—In this paper, a low-voltage CMOS quadrature up-conversion mixer for 5-GHz wireless communication applications is designed. The simulation results demonstrate the mixer can reach a high conversion gain (CG), a low noise figure (NF), and a high linearity (IIP3). A miniature lumped-element microwave broadband rat-race hybrid and RLC shift network are used for the LO and the IF port design, respectively. The mixer exhibits a 3dB improvement in noise and conversion gain, and the image rejection is -35dBc. The mixer achieves noise figure of 12.8 dB, a conversion gain of 15 dB, an output third intercept point at 0dBm, while dissipating 15mW for operating voltage at 1 V. The mixer is designed with TSMC 0.18 um process.

I. INTRODUCTION

The growing demand for portable wireless communication products have driven extensive effort to develop low-voltage and low-cost solutions. Since a few years, a lot of effort has been spent on integrated CMOS systems as a major cost reduction can be realized by minimizing the number of external components and by implementing the different building blocks of the communication system on a single, standard CMOS chip. However, the process scaling reduces the voltage supply. Insufficient voltage headroom causes the RF circuits design to be challengeable and difficult. Hence, low-voltage circuit designs become a crucial issue for current RF and analog circuits design.

Mixer is a key circuit in communication systems. It performs frequency down conversion in a RF receiver and frequency up conversion in a RF transmitter. Its performance directly impacts the whole communications system’s. A commonly used mixer in CMOS systems is the Gilbert mixer [1], shown in Fig. 1. This mixer is made of a differential transconductor, formed by M1 and M2 and a pair of mixer cores, formed by M3-M4 and M5-M6. The transconductor shown is a differential pair, but grounded- source transistors could be used as well. This topology is more suitable for integrated receivers since it requires reduced amount of output filtering.

When up-conversion occurs, two signals are mixed to the same RF frequency. The signal at the LO frequency plus the IF frequency, and the signal at the LO frequency minus the IF frequency, are both mixed to the RF frequency. Besides the desired signal, the image signal is also produced. A common way of avoiding this image problem in fully-integrated transmitter is the use of quadrature up-conversion. In quadrature up-conversion, the IF signal is multiplied by both the in-phase (I) LO signal and a quadrature (Q) LO signal. Using this technique, the image and desired signals remain distinct in the complex RF signal. Usually, a high degree of amplitude and phase matching between the I and Q channels is required to maintain this image rejection. [1][2].

To design a quadrature mixer two Gilberts mixers with the same IF input and quadrature LO signals are often used. The mismatch between the mixer then creates amplitude and phase mismatch between the generated RF signal. It causes the loss of image rejection. If the mixers are operated in the commutating mode, the effect of mismatch in the mixer core is usually negligible, since each transistor operates approximately as a switch [3]. This paper shows the design of a low-voltage ac-coupled mixer with current-reuse technique. This mixer can operate at a supply voltage of 1 V and still offer good performance.
II. THE PRINCIPLE OF MIXER DESIGN

A. Gilbert Cell Mixer

Gilbert Mixer is a double-balanced active mixer [2][3]. Gilbert Mixers are frequently used in RF receivers and transmitters since they can offer conversion gain, high port-to-port isolation and require a smaller LO power [4]. However, they suffer from the noise of the transconductance (M1-M2), switching transistors (M3-M6) and the resistive R. Gilbert mixer is based on the square-law characteristics of the MOS transistor in saturation. This characteristics restricts the linear range of the multiplier to small input voltages. The Gilbert cell has to be modified in order to cancel the quadratic terms originating from the basic MOS device equations for improving linearity and support low voltage operation [2]. The Gilbert cell mixer, usually requires a stack of three transistors and a strong LO voltage. Therefore, the interaction between the transconductance transistors through their common source node leads to substantial third-order nonlinearity degrading the performance[4][5]. In general, the conversion gain of Gilbert Mixer can be expressed as:

\[
\frac{\text{Conversion Gain}}{\text{Gain}} = \frac{2}{\pi} \sqrt{R L}
\]

The double-balanced mixer topology has the advantage of rejecting the strong LO signal and the even-order distortion products. This active mixer has much more relaxed LO requirements. For low-power RFIC design, a smaller LO power becomes necessary. Strong interference to other RF system. Reducing the required LO power also improves the LO-RF and the LO-IF isolation.

Since the double-balanced structure can result effect of virtual ground, Gilbert Mixer has excellent port-to-port isolation. Fig. 2 is used to explain how double-balanced structure benefits the isolation. Besides, compared with passive switch mixer, the switch stage of Gilbert mixer can achieve ideal ON/OFF state by using local oscillator with lower driven. The linearity can be improved by using different degeneration [6]. Ideally, the output of the double balanced mixer transconductance stage is linearly proportional to a differential input, so the linearity is better than that of a single-ended without degeneration.

First we consider the effect of LO-IF leakage. When LO signal wants to interfere IF signal, VG1 point will become virtual ground. Since differential signal LO plus and LO minus will cancel out each other, there will be an excellent isolation between LO signal and IF signal. Identically, LO signal wants to interfere with RF signal on VG2 point, VG2 point will become virtual ground, there will be a excellent isolation between LO signal and RF signal. Therefore, the double-balanced structure has excellent port-to-port isolation.

B. Up-Conversion Mixer

The up-conversion mixers in a quadrature modulator can easily be realized as Gilbert cells [7], with their outputs added in the current domain, shown in Fig. 3. Interestingly, both the linearity of the baseband ports and the phase and gain matching of the mixers impact the quality of the modulated signal. With the assumption that \( \cos \theta \) and \( \sin \theta \) experience third-order distortion. The resulting signal can then be expressed as:

\[
V_{op}(t) = A \alpha \omega_0 [\cos \theta + \cos(3\theta)] - A \alpha \omega_0 [\sin \theta + \sin(3\theta)] \sim (1)
\]

Where \( \alpha \) represents the amount of third-order nonlinearity. \( \alpha \) must be small enough that the transmission mask is not violated. Thus the IF port of the mixers typically incorporates resistive degeneration (Rss) to achieve sufficient linearity.

The matching of up-conversion mixers is also important. Similar to the I/Q mismatch effect in direct-conversion receivers, this imperfection leads to cross-talk between the two data streams modulated on the quadrature phases of the carrier. A common approach to quantifying the I/Q mismatch in a transmitter is to apply two signals \( \cos \omega t \) and \( \cos \omega t \) to the I and Q input terminals and examine the spectrum produced by the adder. In the ideal case, the output in the band of interest is simply given by:

\[
V_{out}(t) = V_o \cos \omega_0 t \cos \omega_0 t - V_o \sin \omega_0 t \sin \omega_0 t
\]

\[
= V_o \cos(\alpha \omega + \alpha \omega) \quad (2)
\]

An unwanted sideband at \( \omega_0 - \omega_0 \) appears at the output. The power of the sideband at \( \omega_0 - \omega_0 \) divided by that of the sideband at \( \omega_0 - \omega_0 \) serves as a measure of the I/Q imbalance. In practice, the crosstalk between the two data streams becomes negligible if the above test yields an
unwanted sideband about 30 dB below the desired signal. Formula (2) could be presented by spectrum analysis, shown in Fig. 4.

C. Microwave Hybrid [8]

In this paper, a microwave hybrid was designed to generate the four-phase split signals for this quadrature up-conversion mixer testing. The signal frequency of IF is set at 10 MHz. This four-phase LO signal generator was designed with ADS Momentum and Ansoft HFSS. Similar results were obtained from these two EM simulators. The topology of this four-phase signal generator is shown in Fig. 5. Fig. 6-a shows the distortion loss of the four-phase signals. From this figure we can see the distortion loss of S21, S31, S41, and S51 are below -7.1dB. The isolation is below -30dB. The phase shift of S21, S31, S41, and S51 are almost ninety degree for a wide frequency range. The simulation results is shown in Fig. 6-b.

III. CURRENT REUSE TECHNOLOGY

In the case of the double balanced mixer, the single NMOS transistor is used as the transconductor. Fig.7 shows four different transconductors suitable for application in the low-voltage quadrature mixer. Actually, they represent improvement of the single NMOS transconductor with respect to operation at low supply voltage.

The transconductor with resistive load is the most simple modification of the single NMOS transconductor [see Fig. 7(a)]. The ac current $I_n$, which is generated in the NMOS transistor, splits to the currents flowing through the switching stage $I_s$ and through the resistor R ($I_r$). The fact that a part of the ac current flows through the resistor R represents the drawback of this transconductor. In order to reduce $I_r$ the value of the resistor R has to be increased. As a consequence care must be taken to keep the dc voltage at the node A sufficiently high in order to keep the transistor M1 saturated. At low supply voltages this problem is even more prominent.

The drawback of the transconductor with resistive load can be alleviated by using the transconductor with active load [see Fig. 7(b)]. By replacing the resistor R with the PMOS transistor the ac current through this transistor $I_p$ is further reduced due to the high output impedance of the PMOS transistor. Instead of using PMOS transistor only to increase the impedance between the node A and $V_{dd}$, it can be also used to amplify RF signals. In this way the leakage of the ac current toward the ac ground through the output impedance of the PMOS transistor can be ideally completely avoided. Hence, a CMOS inverter, which is used as the transconductor, is obtained [see Fig. 7(c)].

In the CMOS inverter, the RF signal amplification by PMOS transistor is a result of current reuse principle, the current reuse principle is for the first time introduced by[9].
This is an efficient way to have a high gain and a low noise figure with a low power. The ac current \( I_s \) is equal to the sum of the ac currents \( I_n \) and \( I_p \). Based on that the total transconductance is equal to \( \beta_{mn}+\beta_{mp} \), where \( \beta_{mn} \) is the transconductance of transistor M1 and \( \beta_{mp} \) is the transconductance of transistor of M2. Before going further with a detailed analysis of the switching mixer that uses the CMOS inverter as the transconductor, it is instructive to check the lowest supply voltage that can be applied. It is determined by the threshold voltages (\( V_t \)) and by the overdrive voltage of the transistors M1 and M2. The overdrive voltages of M1 (\( V_{ovn} \)) and M2 (\( V_{ovp} \)) can be calculated using:

\[
V_{ovn} = V_{fdec} - V_t \\
V_{ovp} = V_{dd} - V_{fdec} - V_t
\]

\( V_{fdec} \) is the biasing voltage applied at the gates of the transistors M1 and M2. The minimal required supply voltage which mixer can operate, can be expressed as:

\[
V_{dd,\text{min}} = V_{ov1} + V_{ov2} + 2V_t
\]

In 0.18 \( \mu \)m CMOS process \( V_t \) is in the range of 0.5 V. Hence, the minimum supply voltage must be higher than 1V. In order to overcome the described limitation, the biasing for NMOS and PMOS transistors in the CMOS inverter have to be separated. In this way an ac-coupled complementary transconductor is obtained, shown in Fig. 7(d). Eq. 5 becomes [10]:

\[
V_{dd,\text{min}} = V_{ov1} + V_{ov2} + 2V_t + V_{fdec} - V_{fdecn}
\]

Choosing \( V_{fdecn} \) to be greater than \( V_{fdec} \), \( V_{dd,\text{min}} \) can be reduced.

IV. DESIGN AND SIMULATION RESULTS

A quadrature up-conversion mixer was designed in a TSMC 0.18um CMOS process and simulated using Agilent ADS and Ansoft HFSS. Figure 8 shows the schematic of the quadrature up-conversion mixer. The simulation results show that the optimum LO power for this design is 0dBm, with 1 V bias conditions. The results show that this mixer has a good conversion gain, a reasonable noise figure and low power dissipation.

Figure 9 shows the RF output harmonic spectrum. The image rejection of this mixer is -35 dBc. Fig. 10 shows the conversion gain and input compression point. The conversion gain and P1dB are 14.8 dB and -27 dBm, respectively. The conversion gain and P1dB of post-simulation are 15dB and -26 dBm, respectively. The simulation and post-simulation results are quite close. Fig.11 shows the output third intercept point. The simulated and post-simulated OIP3 are 0dBm and -2dBm, respectively.

![Figure 8 quadrature up-conversion mixer schematic](image)

![Figure 9 RF Spectrum](image)

![Figure 10 CG and P1dB characteristics](image)

![Figure 11 IIP3 and OIP3 characteristics](image)

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Fig. 12 shows the DSB and SSB noise. Fig. 13 shows the sweep Power LO port-to-port isolation. The layout of mixer is shown in Fig. 14. Including the I/O pads, The chip size of mixer is 1.1 x 1.0 mm. The mixer characteristics is summarized in Table 1. The mixer performance comparison with other published papers is listed in Table 2.

<table>
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<th>Process</th>
<th>Freq (GHz)</th>
<th>Vdd (V)</th>
<th>I (mA)</th>
<th>CG (dB)</th>
<th>NF (dB)</th>
<th>IIP3 (dBm)</th>
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<td>6</td>
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<tr>
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<td>1</td>
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V. CONCLUSION

A high gain, low voltage, low power ac-coupled quadrature mixer with current reuse is presented. This mixer is designed and implemented in 0.18-um CMOS technology. The main advantages of the proposed new mixer topology are high voltage gain (15dB), moderate noise figure (12.5dB), moderate linearity (OIP3=0dBm), operation at low supply voltages (Vdd=1V), and simplicity since common-mode feedback is not necessary.

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